What is claimed is:

(Claim 1) 1. A bias generation circuit generating a bias current for a circuit portion containing a plurality of transistors of a low voltage specification, said circuit portion operating using a first supply voltage, wherein said first supply voltage is greater than said low voltage specification, said bias generation circuit comprising:

a primary current block generating a primary bias current using a second supply voltage, wherein said second supply voltage is less than said first supply voltage;

a backup current block generating a backup bias current using said first supply voltage; and

a multiplexor selecting one of said primary bias current and said backup bias current as said bias current.

(Claim 2) 2. The bias generation circuit of claim 1, wherein said multiplexor selects said backup bias current as said bias current when said second supply voltage is not present.

(Claim 3) 3. The bias generation circuit of claim 2, wherein said multiplexor performs said selecting according to a select signal connected to a node, wherein said primary current block comprises a first current source and said backup current block comprises a second current source, wherein said first current source and said second current source drive said node.

(Claim 4) 4. The bias generation circuit of claim 3, wherein said second current source comprises:

a resistor connected between said first supply voltage and a first node;

a first NMOS transistor; and

a second NMOS transistor,

wherein the drain terminal of said first NMOS transistor is connected to each of said first node and the gate terminal of said first NMOS transistor,

the drain terminal of said second NMOS transistor is connected to said node,

the gate terminal of said first NMOS transistor is connected to the gate terminal of said second NMOS transistor, and

the source terminal of each of said first NMOS transistor and said second NMOS transistor are connected to ground.

(Claim 5) 5. The bias generation circuit of claim 4, further comprising a current mirror circuit which receives said primary bias current generated by said first current source and provides said primary bias current at said node.

(Claim 6) 6. A device comprising:

a processor generating a plurality of digital data elements;

a digital to analog converter (DAC) converting said plurality of digital data elements into an analog signal;

a filter performing a filtering operation on said analog signal to generate a filtered signal; and

a line driver driving a transmission line based on said filtered signal, said line driver comprising a circuit portion and a bias generation circuit, said bias generation circuit generating a bias current for said circuit portion, said circuit portion containing a plurality of transistors of a low voltage specification, said circuit portion operating using a first supply voltage, wherein said first supply voltage is greater than said low voltage specification, said bias generation circuit comprising:

a primary current block generating a primary bias current using a second supply voltage, wherein said second supply voltage is less than said first supply voltage;

a backup current block generating a backup bias current using said first supply voltage; and

a multiplexor selecting one of said primary bias current and said backup bias current as said bias current.

(Claim 7) 7. The device of claim 6, wherein said multiplexor selects said backup bias current as said bias current when said second supply voltage is not present.

(Claim 8) 8. The device of claim 7, wherein said multiplexor performs said selecting according to a select signal connected to a node, wherein said primary current block comprises a first current source and said backup current block comprises a second current source, wherein said first current source and said second current source drive said node.

(Claim 9) 9. The device of claim 8, wherein said second current source comprises:

a resistor connected between said first supply voltage and a first node;

a first NMOS transistor; and

a second NMOS transistor,

wherein the drain terminal of said first NMOS transistor is connected to each of said first node and the gate terminal of said first NMOS transistor,

the drain terminal of said second NMOS transistor is connected to said node,

the gate terminal of said first NMOS transistor is connected to the gate terminal of said second NMOS transistor, and

the source terminal of each of said first NMOS transistor and said second NMOS transistor are connected to ground.

(Claim 10) 10. The device of claim 9, further comprising a current mirror circuit which receives said primary bias current generated by said first current source and provides said primary bias current at said node.

(Claim 11) 11. A method of generating a bias current for a circuit portion containing a plurality of transistors of a low voltage specification, said circuit portion operating using a first supply voltage, wherein said first supply voltage is greater than said low voltage specification, said method comprising:

generating a primary bias current using a second supply voltage, wherein said second supply voltage is less than said first supply voltage;

generating a backup bias current using said first supply voltage; and

selecting one of said primary bias current and said backup bias current as said bias current.